**I2C Register Pin Maps**

**Module Configuration Registers:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I2C\_PSC Values for 12 MHz ICLK** | | | | | | | | | |
| **Field** | **RESERVED** | **PSC** | | | | | | | |
| **Bits** | **31-8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Decimal** | 0 | 3 | | | | | | | |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| **Write**  **Hex** | 0 | 0 | | | | 3 | | | |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I2C\_SCLL Values for 5us tLOW** | | | | | | | | | |
| **Field** | **RESERVED** | **SCLL** | | | | | | | |
| **Bits** | **31-8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Decimal** | 0 | 53 | | | | | | | |
| **Write**  **Binary** | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| **Write**  **Hex** | 0 | 3 | | | | 5 | | | |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I2C\_SCLH Values for 5us tHIGH** | | | | | | | | | |
| **Field** | **RESERVED** | **SCLH** | | | | | | | |
| **Bits** | **31-8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Decimal** | 0 | 55 | | | | | | | |
| **Write**  **Binary** | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| **Write**  **Hex** | 0 | 3 | | | | 7 | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I2C\_OA Values for Master Address** | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **RESERVED** | **OA** | | | | | | | | | |
| **Bits** | **31-12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **Write**  **Hex** | 0 | 0 | | | | 0 | | | | 1 | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Initial Settings for I2C\_CON to bring out of Reset** | | | | | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **I2C\_EN** | **RESERVED** | **OPMODE** | | **STB** | **MST** | **TRX** | **XSA** | **XOA0** | | **XOA1** | | **XOA2** | | **XOA3** | | **RESERVED** | | **STP** | **STT** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | | **7** | | **6** | | **5** | | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | | 0 | | 0 | | 0 | 0 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 8 | | | | 0 | | | | | 0 | | | | | | | 0 | | | |

**Initialization Registers:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Write value to I2C\_CON for Master Transmitter Mode** | | | | | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **I2C\_EN** | **RESERVED** | **OPMODE** | | **STB** | **MST** | **TRX** | **XSA** | **XOA0** | | **XOA1** | | **XOA2** | | **XOA3** | | **RESERVED** | | **STP** | **STT** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | | **7** | | **6** | | **5** | | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | 0 | | 0 | | 0 | | 0 | 0 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 8 | | | | 4 | | | | | 0 | | | | | | | 0 | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Initialization Settings for I2C\_IRQENABLE\_SET Register (All disabled if POLLING)** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **XDR\_IE** | **RDR\_IE** | **RESERVED** | **ROVR** | **XUDF** | **AAS\_IE** | **BF\_IE** | **AERR\_IE** | **STC\_IE** | **GC\_IE** | **XRDY\_IE** | **RRDY\_IE** | **ARDY\_IE** | **NACK\_IE** | **AL\_IE** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 0 | | | | 0 | | | | 0 | | | | 0 | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Initialize Values for I2C\_BUF Register (NO DMA)** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RDMA\_EN** | **RXFIFO\_CLR** | **RXTRSH** | | | | | | **XDMA\_EN** | **TXFIFO\_CLR** | **TXTRSH** | | | | | |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write Decimal** |  | | | 0 | | | | | |  | | 0 | | | | | |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 0 | | | | 0 | | | | 0 | | | | 0 | | | |

**Pre-Transmission Registers:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I2C\_SA Values for Slave Address** | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **RESERVED** | **SA** | | | | | | | | | |
| **Bits** | **31-12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 0 | | | | 7 | | | | 8 | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Initialization Settings for I2C\_CNT Register (Interrupts in use)** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **DCOUNT** | | | | | | | | | | | | | | | |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Decimal**  **Write** | **0** | **To be set before each transmission (dependent)** | | | | | | | | | | | | | | | |
| **Write**  **Binary** | 0 | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? |
| **Write**  **Hex** | 0 | ? | | | | ? | | | | ? | | | | ? | | | |

**Initiate Transmission Registers:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Read Mask Value to read BB from I2C\_IRQSTATUS\_RAW Register (Doesn’t matter if interrupts are enabled)** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **XDR** | **RDR** | **BB** | **ROVR** | **XUDF** | **AAS** | **BF** | **AERR** | **STC** | **GC** | **XRDY** | **RRDY** | **ARDY** | **NACK** | **AL** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Read**  **Binary** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Read**  **Hex** | 0 | 1 | | | | 0 | | | | 0 | | | | 0 | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Start/Stop Condition write on I2C\_CON to initiate transfer** | | | | | | | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **I2C\_EN** | **RESERVED** | **OPMODE** | | **STB** | **MST** | **TRX** | **XSA** | **XOA0** | | **XOA1** | | **XOA2** | | **XOA3** | | **RESERVED** | | | **STP** | | **STT** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | | **7** | | **6** | | **5** | | **4** | | **3** | **2** | | **1** | **0** |
| **Write**  **Binary** | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | 0 | | 1 | 1 |
| **Write**  **Hex** | 0 | 8 | | | | 6 | | | | | 0 | | | | | | | | 3 | | | | |

**Receive Data Registers:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Read Mask Value to read RRDY from I2C\_IRQSTATUS\_RAW Register (Doesn’t matter if interrupts are enabled)** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **XDR** | **RDR** | **BB** | **ROVR** | **XUDF** | **AAS** | **BF** | **AERR** | **STC** | **GC** | **XRDY** | **RRDY** | **ARDY** | **NACK** | **AL** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Read**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **Read**  **Hex** | 0 | 0 | | | | 0 | | | | 0 | | | | 8 | | | |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Read from I2C\_DATA Access Register** | | | | | | | | | |
| **Field** | **RESERVED** | **DATA** | | | | | | | |
| **Bits** | **31-8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Read**  **Binary** | 0 | ? | ? | ? | ? | ? | ? | ? | ? |
| **Read**  **Hex** | 0 | ? | | | | ? | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clear RRDY flag using I2C\_IRQSTATUS Register** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **XDR** | **RDR** | **BB** | **ROVR** | **XUDF** | **AAS** | **BF** | **AERR** | **STC** | **GC** | **XRDY** | **RRDY** | **ARDY** | **NACK** | **AL** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 0 | | | | 0 | | | | 0 | | | | 8 | | | |

**Transmit Data Registers:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Read Mask Value to read XRDY from I2C\_IRQSTATUS\_RAW Register (Doesn’t matter if interrupts are enabled)** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **XDR** | **RDR** | **BB** | **ROVR** | **XUDF** | **AAS** | **BF** | **AERR** | **STC** | **GC** | **XRDY** | **RRDY** | **ARDY** | **NACK** | **AL** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Read**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| **Read**  **Hex** | 0 | 0 | | | | 0 | | | | 1 | | | | 0 | | | |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Write to I2C\_DATA Access Register** | | | | | | | | | |
| **Field** | **RESERVED** | **DATA** | | | | | | | |
| **Bits** | **31-8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | ? | ? | ? | ? | ? | ? | ? | ? |
| **Write**  **Hex** | 0 | ? | | | | ? | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clear XRDY flag using I2C\_IRQSTATUS Register** | | | | | | | | | | | | | | | | | |
| **Field** | **RESERVED** | **RESERVED** | **XDR** | **RDR** | **BB** | **ROVR** | **XUDF** | **AAS** | **BF** | **AERR** | **STC** | **GC** | **XRDY** | **RRDY** | **ARDY** | **NACK** | **AL** |
| **Bits** | **31-16** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **Write**  **Binary** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| **Write**  **Hex** | 0 | 0 | | | | 0 | | | | 1 | | | | 0 | | | |